PCM-3724

PC/104 48-bit Digital I/O Module

User Manual

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CE Notification

PCM-3724 developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

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Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

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- Step 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (OS, version, software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x PCM-3724
- 1 x CD-ROM
- 1 x Startup Manual

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- 1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- 2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

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General Information

Chapter 1 General Information

1.1 Introduction

The PCM-3724 is a PC/104-standard DIO module which attaches to the piggyback connector on your CPU card or PC/104 CPU module. The PCM-3724's two Intel 8255 PPI compatible chips provide 48 bits of parallel digital input/output. Buffered inputs and outputs offer high driving capacity.

The modules's 48 bits are divided into six 8-bit I/O ports: A0, B0, C0, A1, B1 and C1. You can configure each port as either an input or output in software. The module also offers two hardware interrupt lines to the PC.

The module offers two 50-pin OPTO-22 compatible connectors which can connect to a PCLD-7216 SSR I/O module carrier board, PCLD-885 power relay output board, PCLD-785B 24/16-channel relay output board or a PCLD-782B 24/16 channel opto-isolated DI board.

1.2 Features

- 48 TTL digital I/O lines
- · Output status read-back
- Channels simulate 8255 PPI mode 0
- Interrupt triggering, rising/falling edge
- Buffer circuit for high driving capacity, TTL level
- OPTO-22 compatible 50-pin connectors

1.3 Applications

- Industrial AC/DC I/O devices monitoring and controlling
- Relay and switch monitoring and controlling
- · Parallel data transfer
- TTL, DTL and CMOS logic signal sensing
- Indicator LED driving

1.4 Specifications

I/O Channels	48 digital I/O lines
Programming Mode	8255 PPI mode 0
Input Signal	Logic level 0: 0.8 V max. @ -1 μA Logic level 1: 2.0 V min. @ 1 μA
Output Signal	Logic level 0: 0.4 V max. @ 35 mA max. Logic level 1: 2.0 V min. @ -35 mA max.
Driving Capacity	15 LS TTL
Power Consumption	5 V @ 90 mA
Operating Temperature	0 ~ 60°C (32 ~ 140°F) (refer to IEC 68-2-1, 2)
Storage Temperature	-40 ~ 85°C (-40 ~ 185°F)
Operating Humidity	0 ~ 90% RH non-condensing (refer to IEC 68-2-3)
Connector	2x 50-pin box headers
Dimensions	96 x 90 mm (3.8" x 3.5")

1.5 Pin Assignments (J3 and J4)

- 1				(1)			
PC07	1	2	GND	PC17	1	2	GND
PC06	3	4	GND	PC16	3	4	GND
PC05	5	6	GND	PC15	5	6	GND
PC04	7	8	GND	PC14	7	8	GND
PC03	9	10	GND	PC13	9	10	GND
PC02	11	12	GND	PC12	11	12	GND
PC01	13	14	GND	PC11	13	14	GND
PC00	15	16	GND	PC10	15	16	GND
PB07	17	18	GND	PB17	17	18	GND
PB06	19	20	GND	PB16	19	20	GND
PB05	21	22	GND	PB15	21	22	GND
PB04	23	24	GND	PB14	23	24	GND
PB03	25	26	GND	PB13	25	26	GND
PB02	27	28	GND	PB12	27	28	GND
PB01	29	30	GND	PB11	29	30	GND
PB00	31	32	GND	PB10	31	32	GND
PA07	33	34	GND	PA17	33	34	GND
PA06	35	36	GND	PA16	35	36	GND
PA05	37	38	GND	PA15	37	38	GND
PA04	39	40	GND	PA14	39	40	GND
PA03	41	42	GND	PA13	41	42	GND
PA02	43	44	GND	PA12	43	44	GND
PA01	45	46	GND	PA11	45	46	GND
PA00	47	48	GND	PA10	47	48	GND
+5V	49	50	GND	+5V	49	50	GND
6			į.				-

Installation

Chapter 2 Installation

2.1 Initial Inspection

Before starting to install the PCM-3724, make sure there is no visible damage on the card. We carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order on receipt.

As you unpack the PCM-3724, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or fails to meet its specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

2.2 Unpacking

The PCM-3724 contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCM-3724 card from its protective packaging by grasping the card's rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, please store the card in this package for its protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

2.3 Jumper Settings

The PCM-3724 has been designed with ease-of-use in mind. It has one function switch and six jumper setting. The following sections tell how to configure the module. You may want to refer to the figure below for help identifying module components.

Note: Do not install or remove the PCM-3724 I/O board while the power is ON, as this may damage the plug-in board or CPU card.

The following diagram shows the location of the module's switches and jumpers:

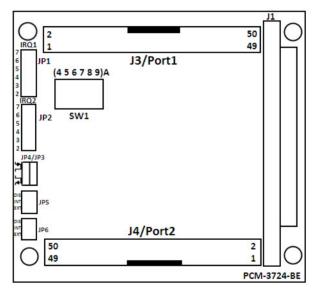


Figure 2.1: Location of Connectors and Jumpers

Base address selection (SW1)

You control the PCM-3724's operation by reading or writing data to the PC's I/O (input/output) port address. The module requires 16 consecutive address locations. Switch SW1 sets the modules's base (beginning) address. Valid base address range from Hex 000 to Hex 3F0. Other devices in your system may, however, be using some of these addresses.

We set the PCM-3724 for a base address of Hex 300 at the factory. If you need to adjust it to some other address range, set SW1 as show below:

Module I/O addresses (SW1)									
Range (hex)	Switch Position								
	1 2 3 4 5 6								
000-00F	•	•	•	•	•	•			
010-01F	•	•	•	•	•	0			
200-20F	0	•	•	•	•	•			
210-21F	0	•	•	•	•	0			
300-30F	0	0	•	•	•	•			
3F0-3FF	0	0	0	0	0	0			
O =Off	On	* =	defaul	t					
Switches 1-6 control the	Switches 1-6 control the PC bus address lines as follows:								
Switch	1	2	3	4	5	6			
Line	A9	A8	A7	A6	A5	A4			

Interrupt settings (JP1, JP2)

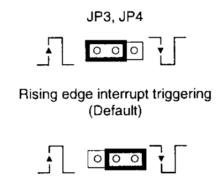
Jumpers JP1 and JP2 control the IRQ levels, as shown below:

JP1 (P	(C00)	JP2 (F	°C1	0)
IRQ 2	0 0	IRQ 2	0	0
3	0 0	3	0	0
4	0 0	4	0	0
5	0 0	5	0	0
6	0 0	6	0	0
7	0 0	7	0	0
(Defa	ault)	(Defa	ault)

Note: You must set each I/O line to a different interrupt level.

Interrupt level (JP3, JP4)

Jumpers JP3 and JP4 select the trigger edge (rising or falling) for I/O lines PC00 and PC10, respectively. Jumpers setting appear below:

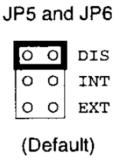


Falling edge interrupt triggering

If you set the PCM-3724 to trap on a rising edge, the module will generate an interrupt if the I/O line (PC00 or PC10) changes from TTL LOW to TTL HIGH. Conversely, if you set the module to trap on a falling edge change, then it will generate an interrupt when the I/O line changes from TTL HIGH to TTL LOW.

Interrupt mode (JP5, JP6)

The PCM-3724 provides two I/O lines (PC00 and PC10) which you can use to generate hardware interrupts to the PC. Jumper JP5 controls interrupt line PC00, and jumper JP6 controls interrupt line PC10. The DIS setting for each jumper (shown in the figure below) disables the corresponding line's interrupt capability. The INT setting enables the line's interrupt capability.



The EXT setting allows you to enable and disable control by external interrupt. I/O line PC04 controls the interrupt on line PC00, and line PC14 controls the interrupt on line PC10. Bring line PC04 to TTL LOW to enable the interrupt capability on PC00. Send line PC04 to TTL HIGH to disable the interrupt capability on PC00. I/O line PC14 controls PC10 in the same way.

2.4 Hardware Installation

- 1. Turn the PC's power off. Turn off the power of any peripheral devices such as printers and monitors.
- 2. Disconnect the power cord and any other cables from the back of the computer.
- 3. Remove the system unit cover (see the users guide for your chassis if necessary).
- 4. Remove the CPU card from the chassis (if necessary) to gain access to the cards PC/104 connector
- Connect connector J1 of the PCM-3724 card to the PC/104 connector. Carefully align the pins with the PC/104 connector. Slide the module into the connector. The module pins may not slide all the way into the connector; do not force the pins into place, or the module may be damaged.
- 6. Fasten the module to the CPU card by using the included brass screw. Screw the brass spacer into the threaded hole on the CPU card. Do not tighten too much, or the threads may be damaged.
- 7. Attach any accessories to the PCM-3724 using 50 pin flat cables.
- 8. Reinstall the CPU card and replace the system unit cover. Reconnect the cables you removed in step 2. Plug in and turn on the power. This completes the hardware installation. Install the software driver as described in the following section.

Operation

Chapter 3 Operation

3.1 Overview

This chapter describes the operating characteristics of the PCM-3724. The driver software bundled with this card allows a user to access all of the card's functions without register level programming. Please see the User's Manual included on the driver CD-ROM for more information. For users who prefer to implement their own bit-level programming to drive the card's functions, information useful for making such a program is included in this chapter.

3.2 Digital I/O Ports

3.2.1 Introduction

The PCM-3724 modules simulate MODE 0 of an Intel 8255 programmable peripheral interface (PPI) chip, with Port C undividable. The module is pin compatible with most industrial solid state I/O racks and modules, such as those manufactured by OPTO-22, Potter Brumfield, Gordos, etc.

The PCM-3724's two 50-pin male IDC connectors interface with directly to OPTO-22 racks. The PCM-3724 offers two I/O lines (PC00 and PC10) to generate hardware interrupts.

3.2.2 8255 Mode 0 Function Definitions

- Mode 0 of the 8255 provides simple input/output functions. No hand-shaking is required since you read or write data directly to or from a specified port.
- Six 8-bit ports (Port A0, B0, C0, A1, B1 and C1)
- Any port can be used for input or output
- Outputs are latched, whereas input are not latched
- The PCM-3724 requires ten I/O ports, identified below:

I/O Port Assignments		
Location	Write	Read
BASE + 0	8255 Port A0	8255 Port A0
BASE + 1	8255 Port B0	8255 Port B0
BASE + 2	8255 Port C0	8255 Port C0
BASE + 3	8255 Mode Register for Ports A0, B0 & C0	N/A
BASE + 4	8255 Port A1	8255 Port A1
BASE + 5	8255 Port B1	8255 Port B1
BASE + 6	8255 Port C1	8255 Port C1
BASE + 7	8255 Mode Register for Ports A1, B1 & C1	N/A
BASE + 8	DIO direction	N/A
BASE + 9	Gate control	N/A

3.2.3 8255 Data Registers

The PCM-3724's I/O ports (BASE+0 to 2 and BASE+4 to 6) directly map to the 8255 ports. Bits assignments for each I/O port appear below:

BASE+0 8255 Port A0 (read/write)											
Bit	7	6	5	4	3	2	1	0			
Value	PA07	PA06	PA05	PA04	PA03	PA02	PA01	PA00			
BASE+1 8255 Port B0 (read/write)											
Bit	7	6	5	4	3	2	1	0			
Value	PB07	PB06	PB05	PB04	PB03	PB02	PB01	PB00			
BASE+	+2 8255	Port C0	(read/w	rite)							
Bit	7	6	5	4	3	2	1	0			
Value	PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00			
BASE+	+4 8255	Port A1	(read/w	rite)							
Bit	7	6	5	4	3	2	1	0			
Value	PA17	PA16	PA15	PA14	PA13	PA12	PA11	PA10			
BASE+	+5 8255	Port B1	(read/w	rite)							
Bit	7	6	5	4	3	2	1	0			
Value	PB17	PB16	PB15	PB14	PB13	PB12	PB11	PB10			
BASE	6 8255	Port C1	(read/w	rite)							
Bit	7	6	5	4	3	2	1	0			
Value	PC17	PC16	PC15	PC14	PC13	PC12	PC11	PC10			

3.2.4 8255 Mode Registers

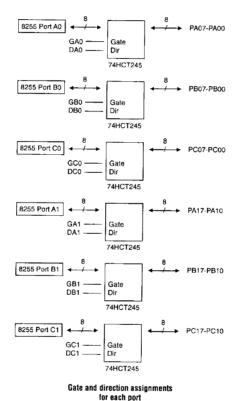
BASE+3 8255 Mode Register Port A0, B0, C0 (write)										
Bit	7	6	5	4	3	2	1	0		
Value	1	0	0	PA0	PC0	0	PB0	PC0		
Where:										
PB0:	PB0: 0= Port B0 as output 1=Port B0 as input									
PC0:	PC0: 0= Port C0 as output 1=Port C0 as input									
PA0: 0= Port A0 as output 1=Port A0 as input										
BASE+7	8255 M	ode Reg	ister Po	ort A1, E	31, C1 (\	write)				
Bit	7	6	5	4	3	2	1	0		
Value	1	0	0	PA1	PC1	0	PB1	PC1		
Where:				•	•			•		
PB1:		B1 as o B1 as in								
PC1: 0= Port C1 as output 1=Port C1 as input										
PA1: 0= Port A1 as output 1=Port A1 as input										
NOTE: After power-on or reset, all ports (Port A0, B0, C0, A1, B1 and C1) are set to input mode.										

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3.2.5 Gate control

Six 74HCT245 chips (one for each port) buffer the PCM-3724's I/O lines to increase driving capacity. Because the 74HCT245 is a bidirectional, tri-state line buffer, you need to set two additional I/O ports (BASE+8 and 9) to control the direction of data flow.

The following diagrams show the gate and direction signals for each port.



Address assignments for the buffer direction register (BASE+8) and gate control register (BASE+9) appear below:

BASE+8 Buffer Direction (write)											
Bit	7	6	5	4	3	2	1	0			
Value	N/A	N/A	DA1	DB1	DC1	DA0	DB0	DC0			
Where:	Where:										
DA0:	0=Port A0 as output 1=Port A0 as input										
DB0:		B0 as ou B0 as in									
DC0:		C0 as ou									
DA1:		A1 as ou A1 as in									
DB1:		B1 as ou B1 as in	•								
DC1:		C1 as ou									
BASE+9	Gate A	ctive/Tri	-state (v	write)							
Bit	7	6	5	4	3	2	1	0			
Value	N/A	N/A	GA1	GB1	GC1	GA0	GB0	GC0			
Where:											
GA0:		A0 rema									
GB0:		B0 rema									
GC0:	0: 0= Port C0 remains tri-state 1=Port C0 becomes active										
GA1:	1: 0= Port A1 remains tri-state 1=Port A1 becomes active										
GB1:	-	t B1 rema B1 beco									
GC1:		t C1 rem C1 beco									

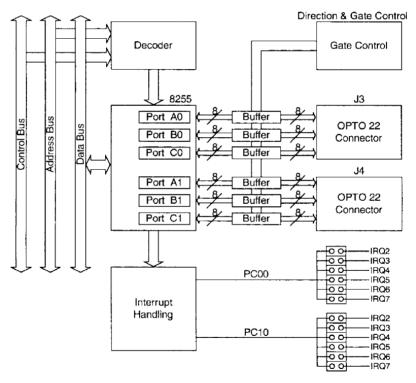
Note: System power-on or reset will clear register BASE+8 and BASE+9, setting all ports to gated-off (tri-state) and input data direction.

3.3 Interrupt Functions

3.3.1 Introduction

The PCM-3724 offers two I/O lines, PC00 and PC10, which you can use to generate a hardware interrupt to the CPU. Interrupts are edge-triggered.

Note: Since the PCM-3724's digital input data are not latched, the module provides no "first event" trapping to determine which input was active first



PCM-3724 Block Diagram

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